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| Substitute for form 1449A/PTO | | | Complete if Known | | |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary) | | | Application Number | Not yet assigned | |
| | | | Filing Date | Herewith | |
| | | | First Named Inventor | GEALER | |
| | | | Group Art Unit | Not yet assigned 2811 | |
| | | | Examiner Name | Not yet assigned | |
| Sheet | 1 | of | 1 | Intel Docket Number | P16923 |

| OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS | | | |
|---|-----------------------|---|----------------|
| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
| me | A | "Integrated Circuit Packages", Copyright(C) FUJITSU LIMITED, 2002, download from http://edevic.fujitsu.com/fj/CATALOG/AD81/81-00001/11e-9.html on 12/4/2003. 1pg. | |
| | B | Lii, Ming-Ji et al: "Flip-Chip Technology on Organic Pin Grid Array Packages", Intel Technology Journal Q3, 2000. 9pgs. | |
| | C | Mahajan, Ravi et al: "The Evolution of Microprocessor Packaging", Intel Technology Journal Q3, 2000. 10pgs. | |
| | D | Intel®: "The Chip Scale Package (CSP)", 2000 Packaging Databook, pages 15-1 – 15-16. | |
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| Examiner Signature | <i>[Signature]</i> | Date Considered | Sep 21. 2005 |
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.